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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/786,204	02/24/2004	Manish Kumar Mathur	2060/US/2	3031

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EXAMINER	
CHO, JAMES HYONCHOL	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 09/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/786,204	MATHUR ET AL.	
	Examiner	Art Unit	
	James Cho	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,9 and 12* is/are rejected.

7)☒ Claim(s) *3,5-8,10 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 February 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to because lines, numbers & letters in Figs. 1 - 6 are not uniformly thick and well defined, clean, durable, and black. 37 CFR 1.84(l). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:
(1) if a machine or apparatus, its organization and operation;
(2) if an article, its method of making;
(3) if a chemical compound, its identity and use;
(4) if a mixture, its ingredients;
(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

The abstract of the disclosure is objected to because of improper content.

Correction is required. See MPEP § 608.01(b).

Claim Objections

Claims 2-3 are objected to because of the following informalities:

"claim 9 " on line 1 of claims 2-3 appears to be --claim 1-- respectively;

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 4, 9 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Lacey et al. (US PAT No. 5,485,107).

Regarding claims 1 and 12, Fig. 4 of Lacey et al. teaches an integrated circuit/a method of operating the input buffer, comprising: at least one pad (DATAOUT) receiving at least one input signal (data output signal); a core (circuit coupled to the output at I/O PAD is inherently required); and at least one input buffer circuit (14'; driver is an input buffer circuit with respect to the receiving end; col. 1, lines 25-33) coupled between said pad and said core, said input buffer having a first mode (operating as a driver by itself; col. 3, lines 37-59) where said input buffer circuit operates as an inverter (14'-19 is an inverter), and a second mode (hot insertion mode; col. 3, line 60 - col. 4, line 60) wherein said input buffer circuit limits the voltage levels within the input buffer (I/O pad is clamped temporarily; col. 4, lines 44-47).

Regarding claim 2, Fig. 4 of Lacey et al. teaches the integrated circuit of claim 19, wherein the first mode includes a normal mode where a supply voltage (Vterm) is applied to said input buffer circuit.

Regarding claim 4, Fig. 4 of Lacey et al. teaches an input buffer circuit having an input (DATAOUT) and a buffer output (I/O PAD), said input buffer operable in a normal mode (col. 3, lines 37-59) and a hot-plug mode (col. 3, line 60 - col. 4, line 60), comprising: a pull-up path (source to drain path of M2) coupled between a first circuit supply (Vterm) and the buffer output (I/O PAD); a pull-down path (source to drain path of M1) coupled between the buffer output (I/O PAD) and a ground reference voltage (ground notation) ; a first transistor (M1) coupled between the input and the pull- up path to activate the pull-up path; a second transistor (M2) coupled between the input and the pull-down path to activate the pull-down path; and a third transistor (M3 keeps M1 off and protects from gliches; col. 4, lines 15-16) for protecting the pull-up path from over-voltage .

Regarding claim 9, Fig. 4 of Lacey et al. teaches the input buffer circuit of claim 4, further comprising: a first bias voltage (voltage at the gate of M2) for biasing the first transistor and a second bias voltage (voltage at the gate of M1) for biasing the second transistor.

Allowable Subject Matter

Claims 3, 5-8 and 10-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Although Lacey et al. (US PAT No. 5,485,107) a backplane driver circuit, one of ordinary skill in the art would not have been motivated to modify the teaching of Lacey et al. to further includes, among other things, the specific of a live-insertion mode where a supply voltage being not applied to the input buffer circuit while an input signal is applied to the at least one pad (claim 3), the input buffer circuit being configured to prevent an over-voltage condition on each of the plurality of transistors (claim 5), a first and second pull-up transistor coupled in series where the second pull-up transistor having a gate biased by the first reference voltage (claim 6), the first bias voltage being approximately 1.1 volts during the normal mode and input minus two diode drops during the hot-plug mode (claim 10), and the second bias voltage being approximately 2.5 volts during the normal mode and approximately the input minus two diode drops during the hot-plug mode (claim 11).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Arai et la. (US PAT No. 6,236,235) discloses an output circuit with a reduced delay and overvoltage protection.

Yeung et al. (US PAT No. 6,346,827) discloses a programmable input/output circuit for a programmable logic device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Cho whose telephone number is 571-272-1802. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James H. Cho
Primary Examiner
Art Unit 2819

8-30-2005